## **REMARKS**

Claims 1-14 are pending in the application, and claims 1-3 and 9-11 stand rejected.

## Rejection under 35 U.S.C §112

Claims 2-8 and 13-14 stand rejected under 35 U.S.C. 112 as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Applicant has amended claims 2, 3, 13 and 14 to address the antecedent basis errors identified by the Examiner, and submits that this rejection may now be withdrawn. Applicant notes that claim 13 has also been amended to clarify a grammatical error, so that the claim now recites "a reference resistor coupled to a base of the output transistor..."

## Rejection under 35 U.S.C §103

Claims 1-3 stand rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 5,831,567 to Seki et al. in view of U.S. Pat. No. 6,281,828 to Kimura et al. In particular, the Examiner finds that Kimura discloses all claimed limitations except for a plurality of reference circuits, each coupled to a respective one of a plurality of comparators, and that Seki discloses an ADC that comprises a plurality of comparators and a plurality of reference circuits where each comparator compares on input electrical signal with a respective pre-selected reference voltage to eliminate DC offset which is contained in the analog signal. The Examiner thus opines that it would have been obvious to the skilled person to modify the reference voltage generator of Kimura by coupling individual reference circuits having pre-selected reference voltages to each comparator as taught by Seki to improve performance and accuracy of the converter. With all due respect, Applicant submits that this conclusion is not supported by the plain language of the two references, and that if the skilled person attempted to combine these two references, the result would not be anticipatory of the present invention.

Kimura addresses the problem inherent in prior art ADCs of equivalent input offset due to device mismatch arising out of the manufacturing process. Kimura attempts to solve this problem by feeding the reference voltage to each comparator through a differential amplifier that

is operated sequentially in two modes (normal and inverted) and the results of which are substracted, to thereby eliminate any signal mismatch due to device mismatch among the various comparators. Kimura does not even mention DC offset in the input analog signal, much less discuss it as being a problem in the ADC that is disclosed. Much more importantly, Kimura requires that the same reference voltage be used through all signal switching sections in order for the disclosed method of inverting and averaging the input analog signal and the reference signal to work. Kimura emphasizes this by disclosing an embodiment that provides multiple reference voltage signals that can be averaged to further reduce possible mismatch error (col. 8, 1l. 3-53). Thus, applying the different reference voltage levels of Seki to Kimura would in fact produce a non-functioning device, and a skilled person attempting to practice the invention of Kimura would never think of applying different reference voltage levels to the different comparator lines.

Furthermore, Seki does not actually disclose an ADC of the type disclosed by Kimura or the type claimed herein. Rather, the device of Seki is aimed at simply providing a binary digital signal R that tracks the frequency of an input analog signal regardless of the DC offset of the input analog signal. It is for this reason that Seki provides the different reference voltage levels V<sub>refi</sub>, as the Examiner has acknowledged. As clear from, *inter alia*, Figs. 15D and 17G, the output signal R of the device of Seki merely tracks the change in phase of the AC component of the amplified input analog signal A. Thus, a skilled person looking to develop or improve an ADC as disclosed by Kimura would not consider applying Seki, as Seki does not in fact disclose a device that provides a digital signal indicative of the <u>magnitude</u> of an input analog signal (i.e. an ADC as typically understood by those skilled in the art and as disclosed by Kimura) but rather indicative of the <u>frequency</u> of the input signal.

In view of the above, Applicant respectfully submits that the two references cited by the Examiner could not be combined together to produce a workable invention, that even if combined the results would not anticipate the present invention, and that there is simply no motivation for the skilled person practicing either reference to consider modifying it by looking to the other. Applicant therefore submits that claim 1 is allowable and respectfully requests the Examiner to reconsider and pass the claim to issue.

Claims 2 and 3 depend from claim 1. "If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious." *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988). Therefore, in light of the above discussion of claim 1, Applicant submits that claims 2 and 3 are also allowable.

## Rejection under 35 U.S.C §102

Claims 9-11 stand rejected under 35 U.S.C. 102(b) as being anticipated by Seki. In particular, the Examiner finds that Seki discloses all of the claimed limitations. Applicant is compelled to respectfully disagree with the Examiner's characterization of this reference. However, in the interest of passing this case to issue, Applicant has amended claim 9 to specifically recite providing each detection signal from each comparator to an encoder arranged to output a signal indicative of a magnitude of the input electrical signal. As explained previously with connection to claim 1, Seki does not output a signal indicative of a magnitude of the input signal, but rather of a frequency of an AC component of the input signal, if such an AC component exists. Applicant therefore respectfully submits that amended claim 9 is patentable over Seki, and respectfully requests the Examiner to reconsider and pass the claim to issue.

Claims 10 and 11 depend from claim 1. In view of the above discussion, it is submitted that claim 9 is now allowable, and for this reason claims 10 and 11 are also allowable.

Applicant acknowledges with gratitude the Examiner's indication of allowability as to claims 4-8 and 12-14. However, in light of the preceding discussion and the amendments made herein, Applicant believes that all claims are allowable.

In view of the above, Applicant submits that the application is now in condition for allowance and respectfully urges the Examiner to pass this case to issue.

The Commissioner is authorized to charge any additional fees which may be required or credit overpayment to deposit account no. 12-0415. In particular, if this response is not timely filed, the Commissioner is authorized to treat this response as including a petition to extend the time period pursuant to 37 CFR 1.136(a) requesting an extension of time of the number of months necessary to make this response timely filed and the petition fee due in connection therewith may be charged to deposit account no. 12-0415.

I hereby certify that this correspondence is being deposited with the United States Post Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on

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(Date of Transmission)

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